

Fig. 5

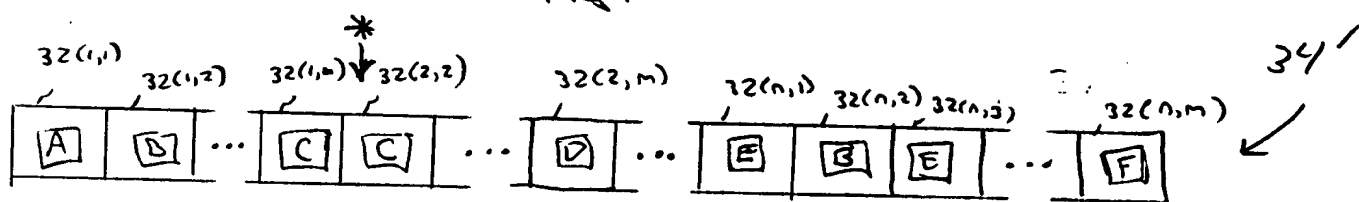


Fig. 6

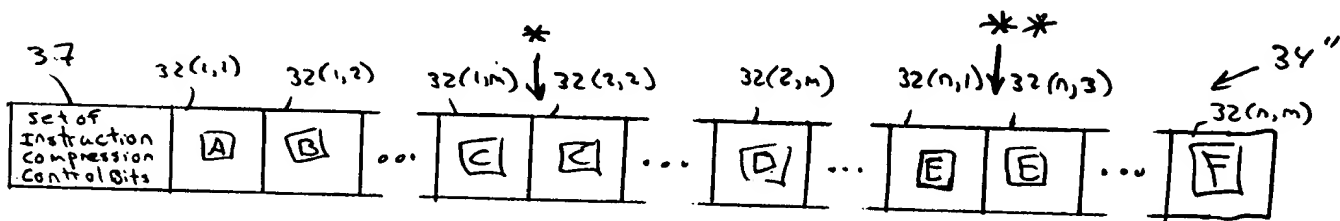


Fig. 7

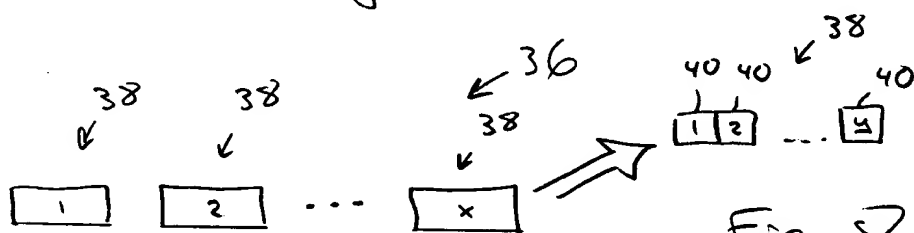


Fig. 8

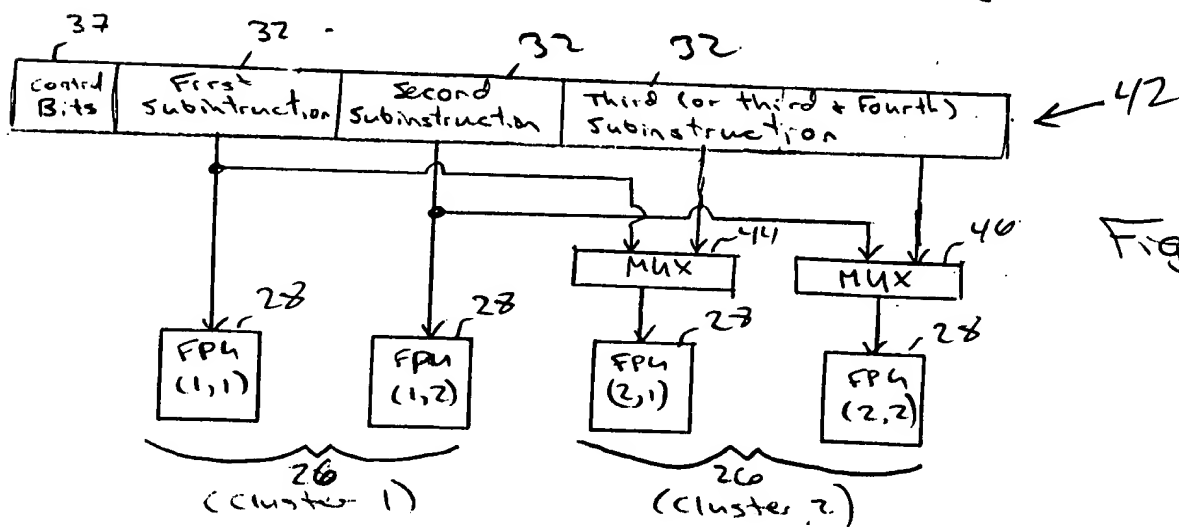
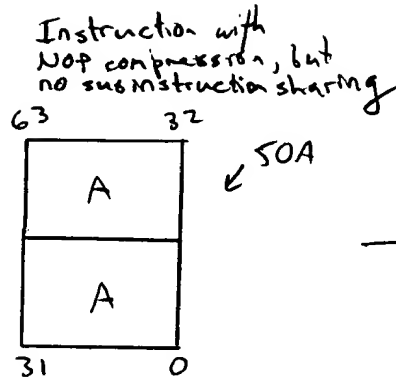
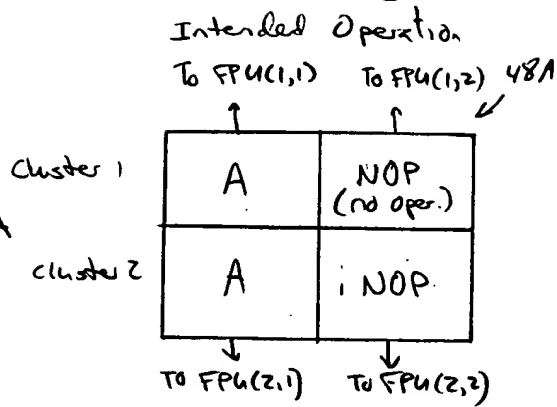


Fig. 9

Fig. 10A



Instruction with subinstruction sharing

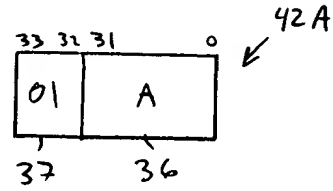


Fig. 10B

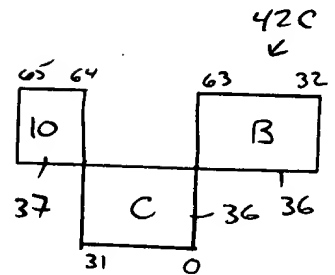
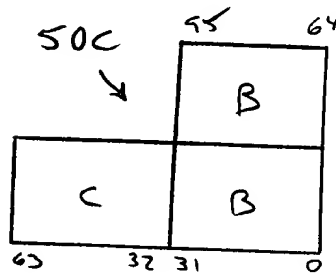
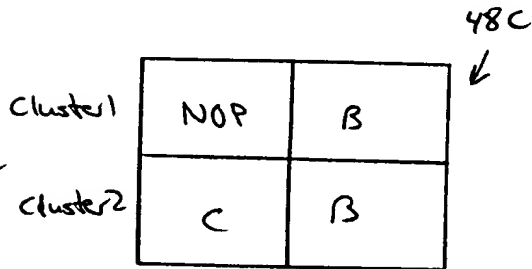
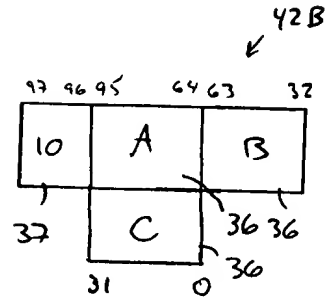
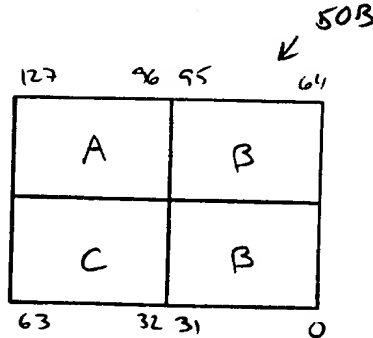
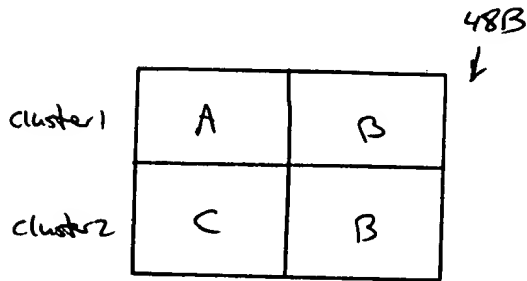


Fig. 10D

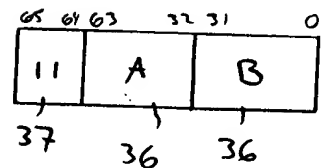
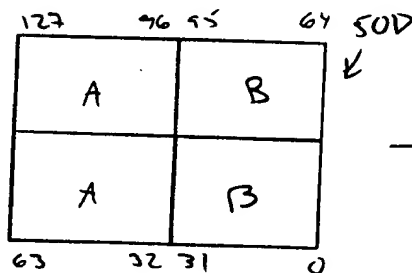
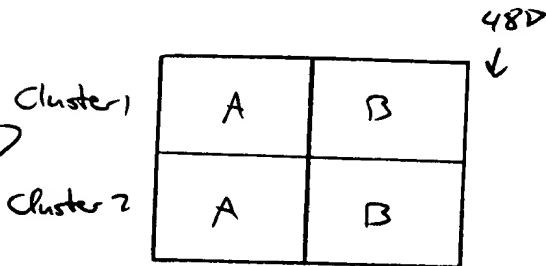
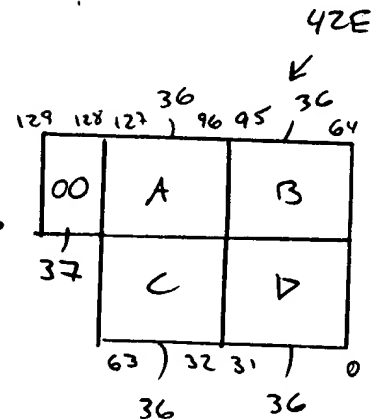
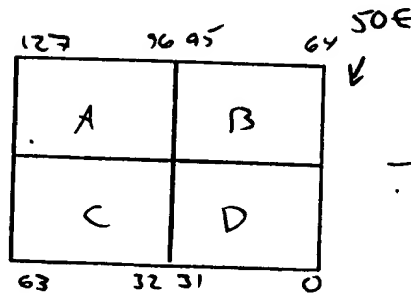
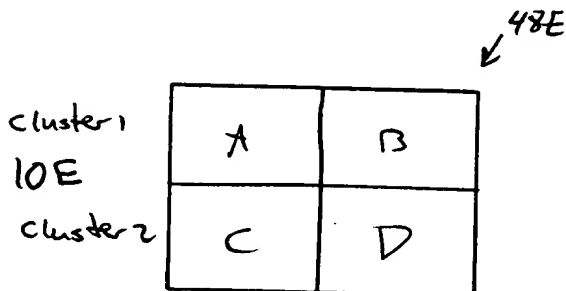


Fig. 10E



```

graph TD
    60([START]) --> 62[Identify subinstruction sharing opportunities]
    62 --> 64[Set Instruction compression Control Bits]
    64 --> 66[Compress Instruction (optional)]
    66 --> 68[store Instruction in Memory]
    68 --> END([END])
  
```

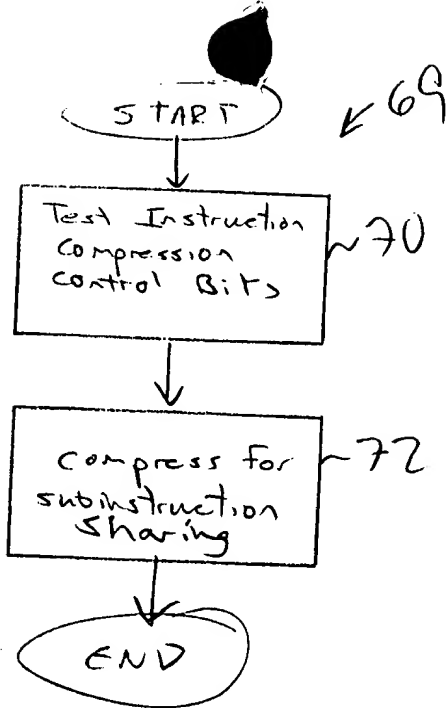
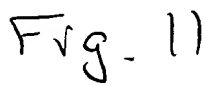


Fig. 12

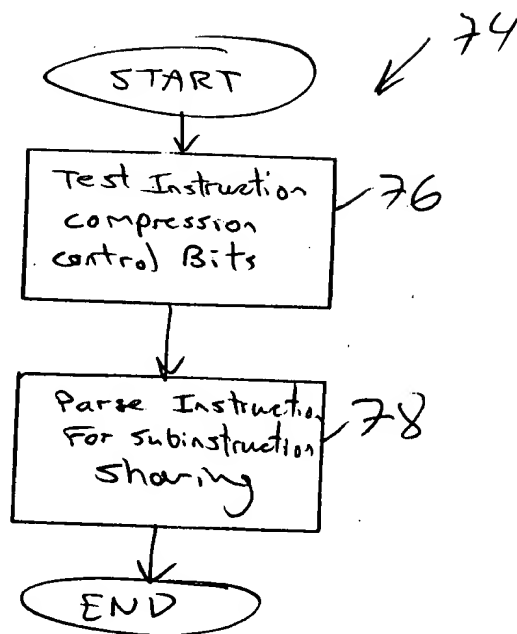


Fig. 13